CSCI-1380: Distributed Computer Systems Homework #1 Assigned: 02/13/2019Due: 02/26/2019

1 Load Balancing and Consistent Hashing

You have a distributed system with which you are using consistent hashing to load balance against. Your ID space is 8 bits long.

- (a) What is the range of IDs that can be supported in this space? Specify you answer in this format "0-N".
- (b) You have the following server IDs: 23, 43, 29, 123, 89, 2. Given this assignment of server IDs. Determine where the following keys will be assigned.

Key ID	Assigned Server
34	
92	
88	
192	
278	
300	

(c) Given the server IDs and the key IDs above, if server with ID 156 were added. Which keys would get assigned to this server?

2 Time: Logical Clocks and Ordering

There are two servers in your system S_1 and S_2 . The two servers generate the following event. Note: e @ 2pm, – indicate the event and the local time of the event at the server.

Process	Events	
S_1 $e_1 @ 1pm, e_2 @ 2pm, e_3 @ 3pm$		
S_2	$e_8 @ 2:10pm, e_9 @ 2:35pm, e_7 @ 2:50pm$	

(a) If the events are processed by the Servers in the order shown in the table below, is the ordering "Total Ordered"? Why?

Process	Events	
S_1	$e_3, e_7, e_9, e_2, e_1, e_8$	
S_2	$e_3, e_7, e_9, e_2, e_1, e_8$	

(b) If the events are processed by the Servers in the order shown in the table below, is the ordering "Total Ordered"? Why?

Process	Events	
S_1	$e_1, e_8, e_9, e_2, e_3, e_7,$	
S_2	$e_1, e_8, e_9, e_2, e_3, e_7,$	

(c) If the events are processed by the Servers in the order shown in the table below, is the ordering "FIFO Ordered"? Why?

Process	Events	
S_1	$e_1 \ e_2 \ e_8, \ e_3, \ e_7, \ e_9$	
S_2	$e_1, e_8, e_2, e_7, e_9, e_3$	

(d) If the events are processed by the Servers in the order shown in the table below, is the ordering "FIFO Ordered"? Why?

Process	Events	
S_1	$e_1, e_2, e_3, e_8, e_9, e_7$	
S_2	e_8,e_9,e_7,e_1,e_2,e_3	

(e) The figure below demonstrates the sequence of events in our simple system. Provide the vector and logical clocks for these events.



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Figure 1: Timeline of events.

Event	Logical Clock	Vector clock
e_1		
e_2		
e_8		
e_3		
e_7		
e_9		