

Processor-Time Tradeoffs under Bounded-Speed Message Propagation: Part I, Lower Bounds

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Abstract

Lower bounds are developed for the processor-time tradeoffs of machines such as linear arrays and two-dimensional meshes, which are compatible with the physical limitation on propagation speed of messages. The machines we consider are characterized by the property that identical numbers of simultaneous memory accesses, operations, and message communications are expressed by the number of processors. For this class of machines, a class of computations is analyzed for which parallelism and locality combined yield speedups superlinear in the number of processors. The results are obtained by means of a novel technique, called the “closed-dichotomy-size technique,” designed to obtain lower bounds to the computation time for networks of processors, each of which is equipped with a local hierarchical memory.